CLAIMS

Please amend the claims as follows.

1. (Currently amended) A data recovery apparatus for a digital data stream of input data, comprising:

phase shifting means for outputting ~~multiple~~a plurality of sampling clocks in a bit time, where the phase of each sampling clock of said plurality of sampling clocks are automatically and independently adjustable;

data sampling means for sampling the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic means for comparing said sampled data signals to said recovered data; and

phase controlling means for estimating the phase relationship between the input data and said plurality of sampling clocks using the comparison result of said compare logic means, and for providing control signals to said phase shifting means according to said estimation results.

2. (Currently amended) The apparatus of claim 1 wherein the phase shifting means comprises:

phase delay means controlled by a first output of said phase controlling means for outputting a first sampling clock of said plurality of sampling clocks using an input clock which is one of an external clock and an internally recovered clock;

first circuit means controlled by a second output of said phase controlling means for outputting a second sampling clock of said plurality of sampling clocks that advances said first sampling clock in phase;

second circuit means controlled by the second output of said phase controlling means for outputting a third sampling clock of said plurality of sampling clocks that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

3. (Original) The apparatus of claim 2, wherein the first circuit means and the second circuit means receive the first sampling clock.

4. (Currently amended) The apparatus of claim 1, wherein the phase shifting means comprises:

a phase distributor outputting a plurality of phase shift values;

a buffer receiving input from the phase distributor and outputting a first sampling clock of the plurality of sampling clocks in accordance with a first output of said phase controlling means; and

selection logic receiving input from the phase distributor and outputting a second and third sampling clock of the plurality of sampling clocks in accordance with a second output of said phase controlling means.

5. (Original) The apparatus of claim 1 wherein the phase shifting means comprises:

a voltage controlled oscillator controlled by a first output of the phase controlling means, circuit means controlled by a second output of said phase controlling means for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

6. (Currently amended) A data recovery apparatus for a digital data stream of input data, comprising:

a phase shifter that outputs ~~multiple~~a plurality of sampling clocks in a bit time, where the phase of each sampling clock of said plurality of sampling clocks are automatically and independently adjustable;

a data sampler that samples the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic that compares said sampled data signals to said recovered data; and

a phase controller that estimating the phase relationship between the input data and said plurality of sampling clocks using the comparison result of said compare logic means, and for providing control signals to said phase shifting means according to said estimation result.

7. (Currently amended) The apparatus of claim 6 wherein the phase shifter comprises:

phase delay logic controlled by a first output of said phase controller for outputting a first sampling clock of said plurality of sampling clocks using an input clock which is one of an external clock and an internally recovered clock;

a first circuit, controlled by a second output of said phase controller, for outputting a second sampling clock that advances said first sampling clock of said plurality of sampling clocks in phase;

a second circuit, controlled by the second output of said phase controller, for outputting a third sampling clock of said plurality of sampling clocks that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

8. (Currently amended) The apparatus of claim 6 wherein the phase shifter comprises:

a voltage controlled oscillator controlled by a first output of the phase controller, a circuit, controlled by a second output of said phase control, for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

9. (Original) A data recovery method for a digital data stream, comprising:

sampling input data at multiple points, where said sampling points are arranged by a predetermined order and adjustable time difference;

providing a first pseudo bit-error signal that is a result of comparison of data sampled at an early boundary with recovered data;

providing a second pseudo bit-error signal that is a result of comparison of data sampled at a late boundary with recovered data; and

using the first and second pseudo bit-error signals, so that the sampling boundary is marginally matched to the edge of an eye opening and one of the intermediate sampling points serves for data recovery.